REMARKS

Claims 1-17 and 21-23 are currently pending in the case. Further examination and reconsideration of the presently claimed application is respectfully requested.

Section 102 Rejections

Claims 1-20 were rejected under 35 U.S.C. § 102(a) as being anticipated by U.S. Patent No. 6,639,831 to Pancholy et al. (hereinafter referred to as "Pancholy"). This rejection is respectfully traversed. A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Bros. v. Union Oil Co. Of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987), MPEP 2131. Pancholy does not disclose all limitations of the currently pending claims, some distinctive limitations of which are set forth in more detail below.

Pancholy does not disclose a memory array with a conductive line having different transistor gates configured to respectively enable read and write operations for different magnetic cell junctions of the memory array. Independent claim 1 recites:

> A memory cell array, comprising: a plurality of magnetic cell junctions and a first conductive line comprising: a gate of a first transistor configured to enable a read operation for one of the plurality of magnetic cell junctions and a gate of a second transistor configured to enable a write operation for another of the plurality of magnetic cell junctions.

Pancholy teaches memory array 60 in Fig. 3 including word line 76 with gates of transistors 78 configured to enable read operations of the array. In addition, memory array 60 includes select line 70 having gates of transistors 68, which are configured to enable write operations of the array. Pancholy, however, fails to disclose either of word line 76 or select line 70 having a transistor gate which is configured to enable an operation opposite than those respectively induced by transistors 78 and 68 for a different magnetic cell junction of memory array 60. In particular, Pancholy fails to disclose word line 76 having a transistor gate which is configured to enable a read operation of memory array 60. In addition, Pancholy fails to disclose select line 70 having transistor gates configured to enable a write operation of memory array 60. Accordingly, Pancholy fails to anticipate the limitations of claim 1.

Pancholy does not disclose a memory array with a bit line spaced apart from a plurality of magnetic cell junctions and further with a series one or more conductive structures coupled between the bit line and one of the plurality of magnetic cell junctions. Independent claim 17 recites:

> A memory array, comprising: a plurality of magnetic cell junctions, a bit line spaced above and arranged in vertical alignment with the plurality of magnetic cell junctions, and a series one or more conductive structures coupled between the bit line and one of the plurality of magnetic cell junctions.

Independent claim 8 recites similar limitations of having a bit line spaced apart from a magnetic cell junction and a set of conductive structures serially coupled thereto. The specification defines a "bit line" on page 2, lines 1-2, as a conductive line that is used for both write and read operations of the array. Although Pancholy teaches conductive lines 24, 44, and 64 in Figs. 1, 2, and 3 may either be arranged in contact or spaced away from adjacent magnetic cell junctions, there is no teaching that such lines are configured for read operations of the cell junctions. Consequently, conductive lines 24, 44, and 64 may not serve as a bit line spaced apart from magnetic cell junctions as recited in claims 8 and 17. Similarly, select lines 30 and 70 and word lines 36 and 76 may not serve as bit lines since none of such lines are used for both write and read operations of a memory array. Pancholy specifically teaches bit lines as conductive lines which are arranged directly in contact with the magnetic cell junctions (see column 1, lines 39-41) and, therefore, bit lines 32 and 86 and bit line bars 34 and 88 cannot be bit lines which are spaced apart from magnetic cell junctions as recited in claims 8 and 17. Such lines are schematically shown spaced apart from the magnetic cell junctions in Figs. 1-3 to differentiate the line from the series of conductive elements 39 coupled to the lower portion of the magnetic cell junction as is commonly done in the art, but there is no teaching within Pancholy that such a spacing physically exists. Consequently, Pancholy fails to anticipate the limitations of claims 8 and 17.

For at least the reasons stated above, Pancholy fails to anticipate the limitations of claims 1, 8, and 17. Therefore, claims 1, 8, and 17, as well as claims dependent therefrom (claims 1, 8, 17, claims 2-7, 9-16, and 18-20), are patentably distinct over the cited art. Accordingly, removal of this rejection is respectfully requested.

CONCLUSION

This response constitutes a complete response to the issues raised in the Office Action Mailed May 4, 2005. The prior art made of record but not relied upon is not considered pertinent to the presently claimed case. In view of the remarks herein traversing the rejections, Applicants assert that pending claims

1-20 are in condition for allowance. If the Examiner has any questions, comments, or suggestions, the undersigned attorney earnestly requests a telephone conference.

No fees are required for filing this amendment; however, the Commissioner is authorized to charge any additional fees, which may be required, or credit any overpayment, to Daffer McDaniel LLP Deposit Account No. 05-3268/5298-17000.

Respectfully submitted,

Kevin L. Daffer
Reg. No. 34,146
Attorney for Applicants

Daffer McDaniel LLP
P.O. Box 684908
Austin, TX 78768-4908
Ph: (512) 476-1400
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